AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Cancelled)

2. (Currently Amended) The semiconductor integrated circuit described in Claim 4 [[1]], further comprising a latch circuit latching the parallel data output from the serial/parallel conversion circuit and supplying the data to the memory.

3. (Currently Amended) The semiconductor integrated circuit described in Claim 4 [[1]], wherein the serial/parallel conversion circuit includes a shift register.

4. (Currently Amended) ~~The semiconductor integrated circuit described in Claim 1,~~

A semiconductor integrated circuit comprising:

a serial/parallel conversion circuit receiving serial data and a clock signal, and outputting parallel data;

a memory storing the parallel data; and

a write pulse producing circuit producing a write pulse setting a time for writing data into the memory by counting clock signals,

wherein the write pulse producing circuit includes:

a counter counting clock signals[[,]];

a first coincidence detecting circuit detecting coincidence between a count value of the counter and a first predetermined value;

a second coincidence detecting circuit detecting coincidence between the count value of the counter and a second predetermined value; and

a sequence circuit producing the write pulse by setting an output level to a first level during a period starting from detection of the coincidence by the first coincidence detecting circuit to detection of the coincidence by the second coincidence detecting circuit and by setting the output level to a second level during a period starting from detection of the coincidence by the second coincidence detecting circuit to detection of the coincidence by the first coincidence detecting circuit.